Features

- SPI for Microcontroller Connection with Up to 1 Mbit/s
- Internal Data Buffer for Timing-independent Data Transmission
- Programmable Driver Current Regulation
- One-chip Antenna Driver Stage for 1A Peak Current
- LF Baud Rates Between 1 kbaud and 4 kbaud
- Quick Start Control (QSC) for Fast Oscillation Build-up and Decay Timing
- Integrated Oscillator for Ceramic Resonators
- Power Supply Range from 7.5V to 16V Direct Battery Input (Up to 28V With Limited Function Range)
- Amplitude Shift Keying (ASK) Modulation
- Phase Shift Keying (PSK) Modulation
- Carrier Frequency Range from 100 kHz to 150 kHz
- Operational Temperature –40°C to +105°C
- EMI and ESD According to Automotive Requirements
- Highly Integrated — Less External Components Required

Applications

- Hands-free Car Access (Passive Entry/Go)
- Tire Pressure Measurement
- Home Access Control
- Care Watch Systems

Benefits

- Diagnosis Function and Overtemperature Protection
- Load Dump Protection Up to 45V for 12V Boards
- Power-down Mode for Minimum Power Consumption

1. Description

The ATA5278 device is an integrated BCDMOS antenna driver IC dedicated as a transmitter for Passive Entry/Go (PEG) car applications and for other hands-free access control applications.

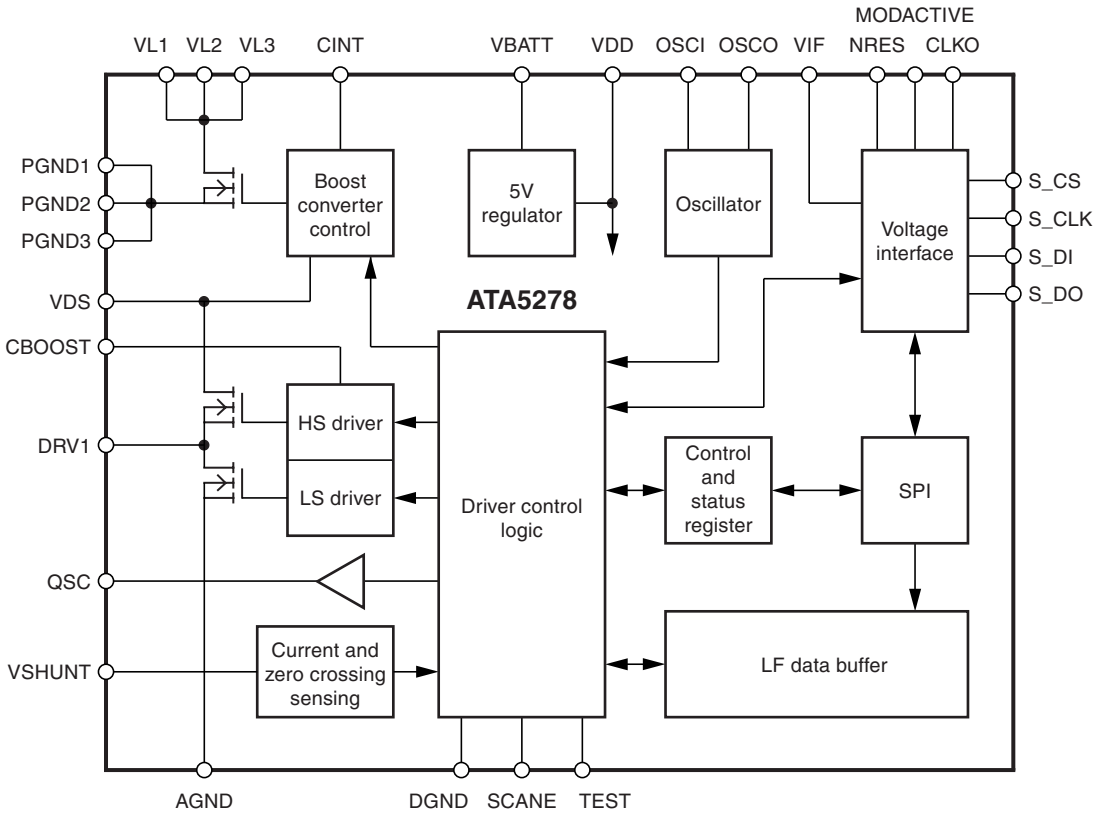
It includes the full functionality of generating a magnetic LF field in conjunction with an antenna coil to transmit data to a receiver in a key fob, card or transponder. A microcontroller can access the chip via a bi-directional serial interface.

Stand-alone Antenna Driver

ATA5278

4832D–RKE–12/07

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN28

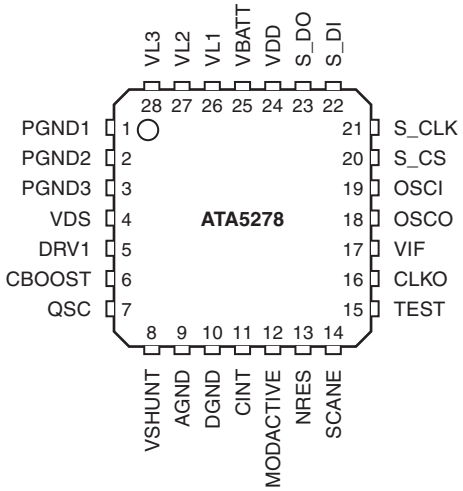


Table 2-1. Pin Description

Pin	Symbol	Function
1	PGND1	Boost transistor ground
2	PGND2	Boost transistor ground
3	PGND3	Boost transistor ground
4	VDS	Driver voltage supply input
5	DRV1	Antenna driver stage output
6	CBOOST	External bootstrap capacitor connection
7	QSC	QSC transistor-gate driver-stage output
8	VSHUNT	Antenna current-shunt resistor connection
9	AGND	Analog ground (sensoric/antenna driver)
10	DGND	Digital ground (logic)
11	CINT	External integrator-capacitor connection
12	MODACTIVE	Modulator status pin output
13	NRES	Reset input (inverted)
14	SCANE	For factory test purposes only (connect to ground)
15	TEST	For factory test purposes only (connect to ground)
16	CLKO	Clock signal output
17	VIF	Logic interface voltage supply
18	OSCO	Oscillator output (for resonator/crystal connection)
19	OSCI	Oscillator input (for external clock source or resonator/crystal connection)
20	S_CS	Chip select for serial interface
21	S_CLK	Clock input for serial interface
22	S_DI	Data input for serial interface
23	S_DO	Data output of serial interface
24	VDD	Internal 5 V stabilizing capacitor connection
25	VBATT	Battery supply
26	VL1	Coil connection for the boost converter low-side switch
27	VL2	Coil connection for the boost converter low-side switch
28	VL3	Coil connection for the boost converter low-side switch

3. Functional Description

3.1 General Description

The IC contains a half-bridge coil driver stage with a special driver voltage regulator and control logic with diagnosis circuitry. It is controllable by a serial programming interface (SPI).

In combination with an LC antenna circuitry, the IC generates an electromagnetic LF field. The carrier frequency for the antenna is generated by the oscillator and a pre-scaler logic.

The LF field can be modulated to transmit data to a suitable receiver. Two modulation modes are available: Amplitude Shift Keying (ASK) and 180° Phase Shift Keying (PSK). The transmission data has to be stored in the internal data buffer.

The IC consists of two main functional blocks:

- The SPI with the data buffer, the control registers and the oscillator
- The driver stage with its control logic and the power supply stage

A boost converter is used to supply the driver half-bridge with a high voltage and a regulated current even if the battery voltage is low. The antenna current is programmable in 16 steps to support a transmission with various field strengths.

The driver circuitry is protected against short-circuits and overload.

3.2 Operational States

After power-on-reset, the ATA5278 is in power-down mode. To achieve minimum power consumption, only the internal 5-V supply and the control registers are active. The IC can only be activated by the external control unit via the serial interface (i.e., the chip select line is enabled).

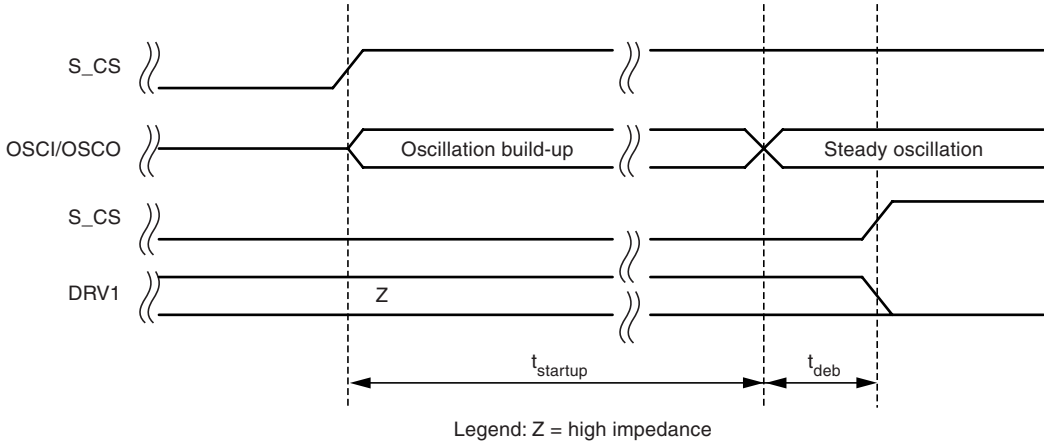
Once activated, the chip keeps the oscillator active and waits for commands on the serial bus. This state can be described as standby mode. Only upon an external reset or on command followed by disabling the chip select line, the power-down mode is re-invoked.

The modulator stage, together with the antenna driver and the power supply, is activated as soon as LF data is written into the buffer and remains in this state until all data has been sent, a stop command has been given via the SPI or a fault occurred. The data modulation is running independently of the SPI activity and can be monitored with the MODACTIVE pin.

3.3 Power-down Mode

The ATA5278 should be kept in power-down mode as long as the LF channel is not used, because not only is the current consumption minimal, but the internal logic is also reset. The antenna driver stage is in high impedance mode. To power-up the chip, the chip-select line (S_CS) has to be activated for an appropriate time. The SPI then starts the internal oscillator which is necessary for proper operation. Only after a certain oscillation build-up time, is full functionality available. The microcontroller can check out the state of the IC with two state bits automatically returned by any SPI command.

Figure 3-1. Power-up Timing

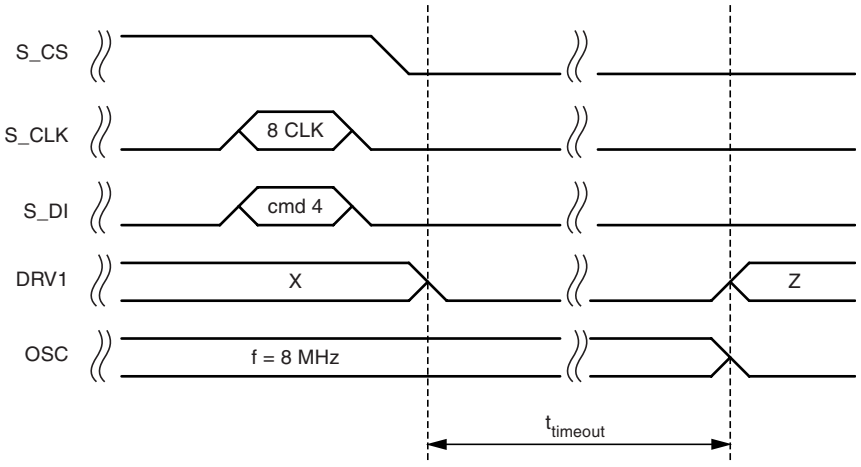


Legend: Z = high impedance

The startup time, $t_{startup}$, in Figure 3-1 depends on the clock source used in the application. Typical oscillation build-up times are below 100 µs for ceramic and about 1 ms for crystal resonators. When using an active clock source, the startup time can be neglected. The internal logic debounces the first clock signals until it finally powers-up the IC for the time t_{deb}. Note that during this time, the chip select signal S_CS has to be permanently active.

The normal way to bring the chip back into power-down mode is to use an SPI command. Deactivating the chip-select line right after the power-down command, an internal standby timer is started and will run for $t_{timeout} = (2048/f_{OSCI})$. In this time, the antenna driver stage is stopped to discharge any energies possibly remaining in the antenna circuit. If the chip-select line is reactivated during this time, the sequence is interrupted and the IC remains in standby mode. Otherwise, the power-down mode is engaged after the timeout, the oscillator is stopped and the driver stages are switched to high impedance. Figure 3-2 illustrates this behavior.

Figure 3-2. Power-down Timing

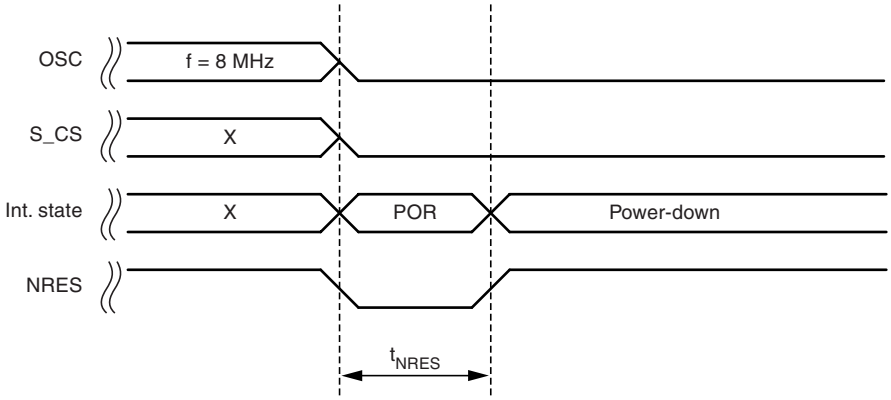


Legend: X = do not care
Z = high impedance

Note that if command 4 is omitted and only the chip-select line is disabled, the ATA5278 stays operational (i.e., the oscillator keeps running, an eventually running LF data modulation is not interrupted). Here, only the SPI itself is disabled and the serial bus can be used for other devices connected to it.

In case the microcontroller is not able to communicate properly with the ATA5278 or any other disturbance has occurred, it can trigger a reset (like a power-on-reset, POR) in the chip by pulling the NRES pin to ground, which will bring the logic back to the startup state, i.e., all configurations are at default and the IC is in power-down mode.

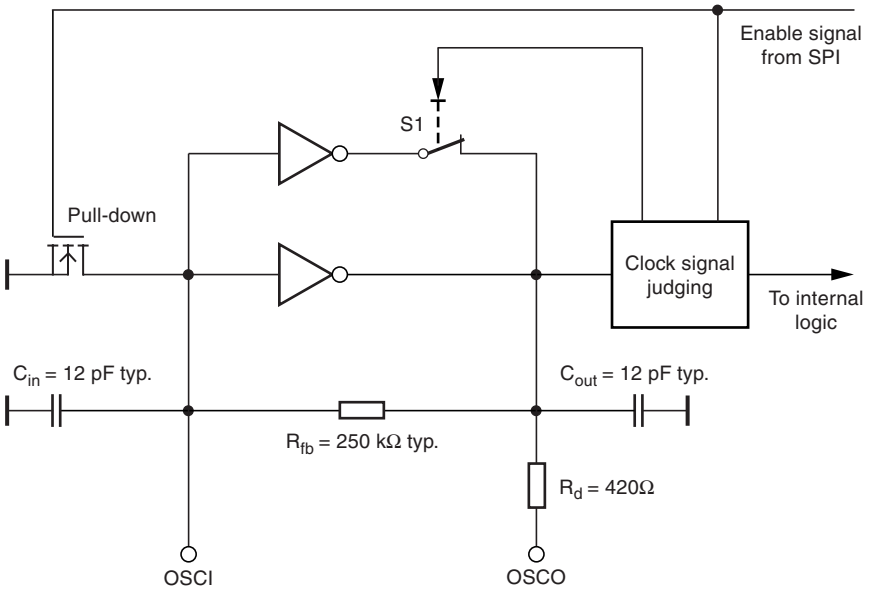
Figure 3-3. External Reset



3.4 Oscillator

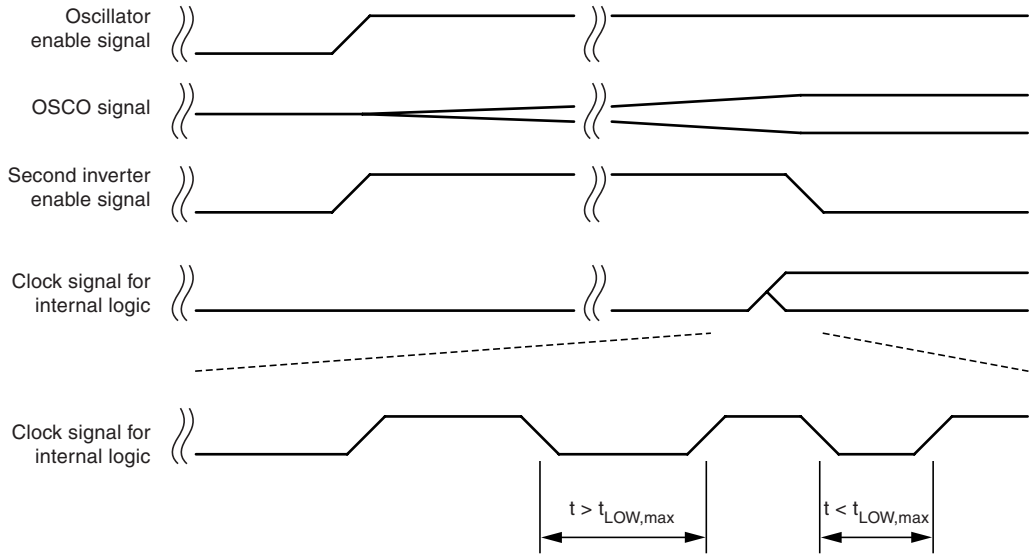
The ATA5278 is equipped with an internal oscillator circuitry that provides the system clock signal needed for operation. It is intended to work with an externally applied passive reference device such as a ceramic resonator or a crystal. Active clock sources like microcontrollers or crystal oscillators, however, can also be used. Figure 3-4 shows the internal structure of the oscillator circuitry.

Figure 3-4. Internal Oscillator Circuitry



The main element of this circuit is the parallel inverting stage which generates the clock signal in conjunction with the external reference device. During power-down mode, these inverters are shut down and the pull-down structure on the OSCI pin is active. As soon as the SPI enables the oscillator, the pull-down is disabled and the inverters are powered up. Now, the clock signal assessment stage monitors the signal on the OSCI pin. As soon as the amplitude and the period reach acceptable values, one of the two inverters (i.e., the drivers) is shut down in order to reduce power dissipation in the external reference device. Figure 3-5 illustrates the period assessment.

Figure 3-5. Oscillator Signal Assessment



3.5 I/O Voltage Interface

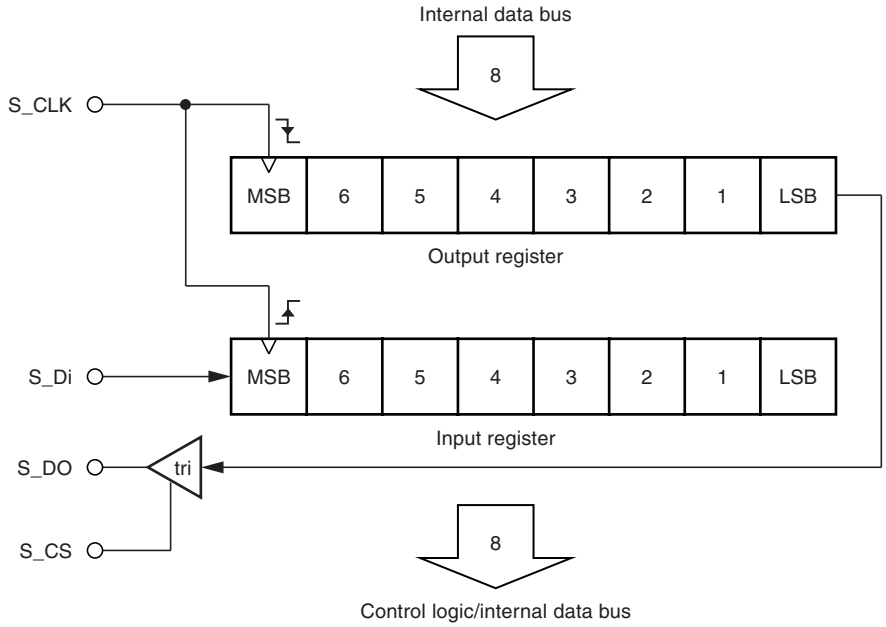
All digital I/O pins, including the reset input pin NRES, are passed through the internal voltage interface before they reach their concerning blocks. This interface prevents possible compensation currents, as the control logic of the ATA5278 is supplied by the internal 5V regulator. It is capable of handling I/O voltages between 3.15V and 5.5V, determined by the voltage applied to the VIF pin.

The pins NRES and S_CS are additionally equipped with a pull-up and a pull-down structure respectively in order to ensure a defined behavior of the ATA5278 in case of a broken connection. If the NRES line is broken, the pull-up structure keeps the input in passive state and normal operation is possible. A broken S_CS line will cause a permanently disabled SPI and S_DO pin, so communication between the microcontroller and other SPI bus members is still possible. For further details on the voltage interface, please refer to the table “Electrical Characteristics” on page 27.

3.6 SPI

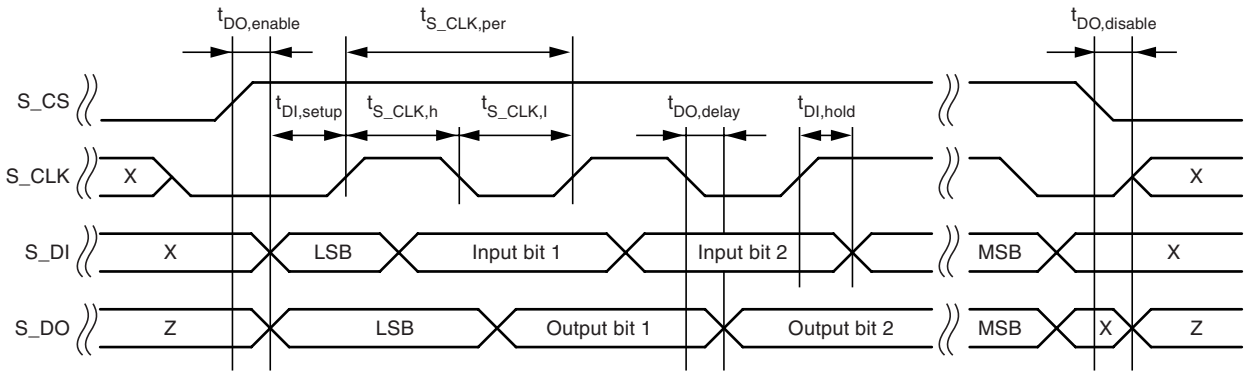
The control interface of the ATA5278 consists of an eight-bit synchronous SPI. It has a clock input (S_CLK) which supports frequencies up to 1 MHz, a chip select line (S_CS) which enables the interface, a serial data input (S_DI) and a serial data output (S_DO). The output pin is of a tristate type, which will be set to high-impedance state as soon as the chip-select line is disabled. The interface is in slave mode configuration. This means that an SPI master (e.g. a microcontroller) is required for communication with the ATA5278, as the IC will neither start a communication by itself nor is it able to provide the serial clock signal. Figure 3-6 sketches the internal structure.

Figure 3-6. SPI Structure

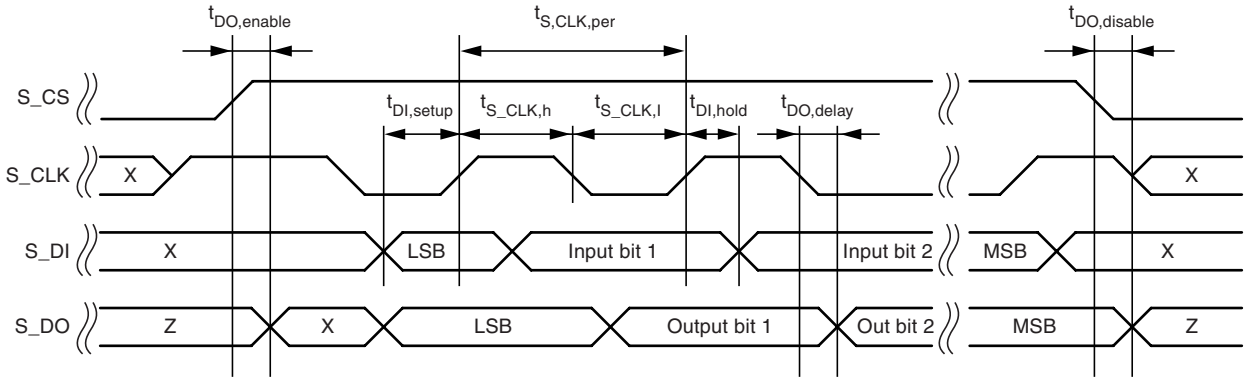


Once enabled by the chip-select line, the data at the S_DI pin is shifted into the input register with every rising edge of the input clock signal. At the pin S_DO, the actual data of the LSB of the output register is available. The output register is shifted on every falling edge of the input clock signal. Two timing schemes for SPI data communication are supported, which are shown in Figure 3-7 on page 9.

Figure 3-7. SPI Timing Diagram



First Possible Serial Timing, S_CLK Polarity 0, Phase 0



Second Possible Serial Timing, S_CLK Polarity 1, Phase 1

3.7 SPI Commands

The microcontroller can access the following functions of the ATA5278 via the SPI:

- Read from/write to configuration register 1
- Read from/write to configuration register 2
- Read from the status register
- Write LF transmission data to the buffer and start the transmission
- Verify the state of the data buffer
- Clear the fault memory
- Stop the modulator
- Enable the power-down mode

Table 3-1 on page 10 lists all functions and their definitions.

Table 3-1. SPI Commands

No.	I/O	MSB	6	5	4	3	2	1	LSB	Description
1	I1 O1	0 SR	0 0	0 0	0 0	0 0	0 0	0 RTS	0 0	Check status of IC SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready
2	I1 O1	0 SR	0 0	0 0	1 0	0 0	0 0	0 RTS	1 0	Reset fault memory SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready
3	I1 O1	0 SR	0 0	1 0	0 0	0 0	0 0	0 RTS	1 0	Stop modulator SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready
4	I1	0 SR	1 0	0 0	0 0	0 0	0 0	0 RTS	1 0	Enable power-down mode SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready
5	I1 O1 I2 O2	0 SR 0 0	0 0 0 0	0 0 IC3 0	0 0 IC2 0	0 0 IC1 0	1 0 IC0 1	0 RTS 0 0	0 0 AP 0	Write configuration register 1 SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready IC3..0: antenna coil current selector AP: 0 ASK modulation mode, 1 PSK modulation mode
6	I1 O1 I2 O2	0 SR X 0	0 0 X 0	0 0 X IC3	0 0 X IC2	0 0 X IC1	1 0 X IC0	1 RTS X 0	0 0 X AP	Read configuration register 1 SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready IC3..0: antenna coil current selector AP: 0 ASK modulation mode, 1 PSK modulation mode
7	I1 O1 I2 O2	0 SR 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 1	0 0 BR1 0	0 RTS BR0 0	0 0 PS 0	Write configuration register 2 SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready BR1..0: LF data baud rate selector PS: 0 CLKO prescaler disabled, 1 prescaler enabled
8	I1 O1 I2 O2	0 SR X 0	0 0 X 0	0 0 X 0	0 0 X 0	1 0 X 0	0 0 X BR1	1 RTS X BR0	0 0 X PS	Read configuration register 2 SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready BR1..0: LF data baud rate selector PS: 0 CLKO prescaler disabled, 1 prescaler enabled
9	I1 O1 I2 O2	0 SR X 0	0 0 X 0	0 0 X IC	0 0 X CH	1 0 X OL	1 0 X SH	1 RTS X SL	0 0 X OT	Read status register SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready IC: illegal command received CH: overcurrent in antenna footpoint detected OL: open load detected SH: overcurrent to VBATT detected at driver output SL: overcurrent to GND detected at driver output OT: overtemperature detected
10	I1 O1 I2 O2	0 SR X 0	0 0 X D6	0 0 X D5	0 0 X D4	0 0 X D3	0 0 X D2	1 RTS X D1	0 0 X D0	Check free LF data buffer space SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready D6..0: free logical LF data bits in buffer
11	I1 O1 Ix Ox	1 SR HB7 B7	D6 0 HB6 B6	D5 0 HB5 B5	D4 0 HB4 B4	D3 0 HB3 B3	D2 0 HB2 B2	D1 RTS HB1 B1	D0 0 HB0 B0	Write LF data to buffer and start modulator SR: 0 system not ready, 1 system ready RTS: 0 modulator not ready, 1 modulator ready D6..0: number of logical LF bits to be written into buffer HB7..0: LF half bits (2 for one logical bit) B7..0: input bit from the previous controller data word

3.8 Command Description

Table 3-1 on page 10 summarizes the commands interpreted by the SPI control logic of the ATA5278. Each command consists of one or more data words which the controller has to transfer to the SPI of the ATA5278. An SPI data word is always eight bits in width and has to be transferred starting with the least significant bit (LSB).

The following list contains detailed information on every command of the chip.

- The main purpose of **command 1** is to check the operational status of the chip. Only if the System-Ready bit (SR) and the Ready-To-Send bit (RTS) have been received as 1, the ATA5278 is fully functional. In special cases, only the SR bit will be received as 1. This is when the LF data buffer is full or when the power stages have been shut down due to a fault. This command can be used at any time to check the status of the chip.
- **Command 2** is the first out of three special function commands. It is used to reset the internal fault memory. Once a fault is detected by the internal diagnosis stage, it is stored in the fault memory (i.e., the status register) and the power stages are shut down to protect them from damage. In order to enable the chip again, this command has to be sent to the IC.
- **Command 3** can be used to stop the LF data transmission immediately. Regularly, the modulator stage works as long as new (i.e., unsent) LF data is in the data buffer. When using this command, all data in the buffer will be deleted and the antenna driver stage is switched to idle mode.
- **Command 4** has to be used to shut down the IC. In order to start the power-down sequence properly, no further command must be transmitted to the chip and the chip-select line (S_CS) has to be disabled afterwards.
- **Command 5** is used to write configuration data into register 1, which is used for LF data modulation control. All register access commands are of a 16-bit structure (i.e., two data words). The first data word defines the access itself (i.e., read or write, and the register number). The second data word is the configuration data, which is to be sent to the ATA5278. Note that in return for the second data word, the first input data word is sent back to the controller. This can be used to validate the SPI transmission. Register 1 contains the four-bit-wide antenna coil current selector (IC3..IC0) and the modulation type selector bit (NASK_PSK). For further details, please refer to the section “Current Adjustment” on page 19.
- **Command 6** can be used to validate a change in register 1 (i.e., a prior command 5 operation) or to check its actual state after a power-down period. Like all register access commands, it consists of two data words. The return data in the second data word has the same bit sequence as in command 5.
- **Command 7** writes configuration data to register 2, which handles timing relevant setup information. Like all register access commands, it consists of two data words, where the second one is the configuration data itself. Note that in return for the second data word, the first input data word is sent back to the controller. This can be used to validate the SPI transmission. Register 2 contains the two-bit-wide LF data baud-rate selector (BR1..BR0) and the pin CLKO prescaler bit. For further details, please refer to the sections “LF Data Modulation” on page 13 and “Clock Supply”.
- **Command 8** can be used to validate a change of register 2 (i.e., a prior command 7 operation) or to check its actual state after a power-down period. Like all register access commands, it consists of two data words. The return data in the second data word has the same bit sequence as in command 7.

- The status register of the ATA5278 can be read out with **command 9**. As soon as the internal diagnosis stage detects a fault, it is stored in the status register until a fault reset command is given or a power-on-reset occurs. Note that the power stages of the chip are disabled as long as a power stage fault (i.e., a short-circuit at the driver stage output pin, open load, overcurrent at the current sense pin or over temperature) is present in the status register. Like all register access commands, it consists of two data words, where the return data in the second data word contains the fault bits. For further details, please refer to the section "Fault Diagnosis" on page 20.
- **Command 10** accesses a special register, where the actual amount of free logical bits in the data buffer is stored. This value decreases with each logical bit that is transferred to the buffer, and increases with each logical bit the modulator stage fetches from the buffer in order to transmit it via the LF channel. It can be used to determine the amount of data which can be transferred to the buffer or to determine the actual modulation process. Like all register access commands, it consists of two data words, where the second one contains the six-bit-wide value.
- **Command 11** is used to write LF data to the on-chip data buffer and to start the modulator stage. This command is indicated by the most significant bit (MSB) of the first data word from the controller, which is, in contrast to all other commands, 1. The other seven bits of this word determine the amount of logical LF data to be written to the buffer. This amount of data has then to be transferred from the controller to the ATA5278. As one logical bit consists of two half bits, a maximum of four logical bits can be transferred per one SPI data word. With the data buffer being able to store up to 96 logical bits, command 11 may reach a maximum length of 25 SPI data words (i.e., the first word with the amount of data, followed by up to 24 words with the data itself). Note that the input data from the SPI input register is always read out starting from the least significant bit (LSB), working towards the MSB. So if less than four logical bits are transferred to the buffer, they have to be stored in the lower area of the SPI data word (i.e., starting with the LSB). It is important that the number of actually transferred LF data matches the amount given in the first word of this command, because there are no consistency checks. This is even then the case if the data buffer was already full at the beginning of the transmission, or got full during the transmission of LF data, or if the driver stages are disabled due to a present fault. Data which is transferred under such circumstances is not stored and therefore lost.

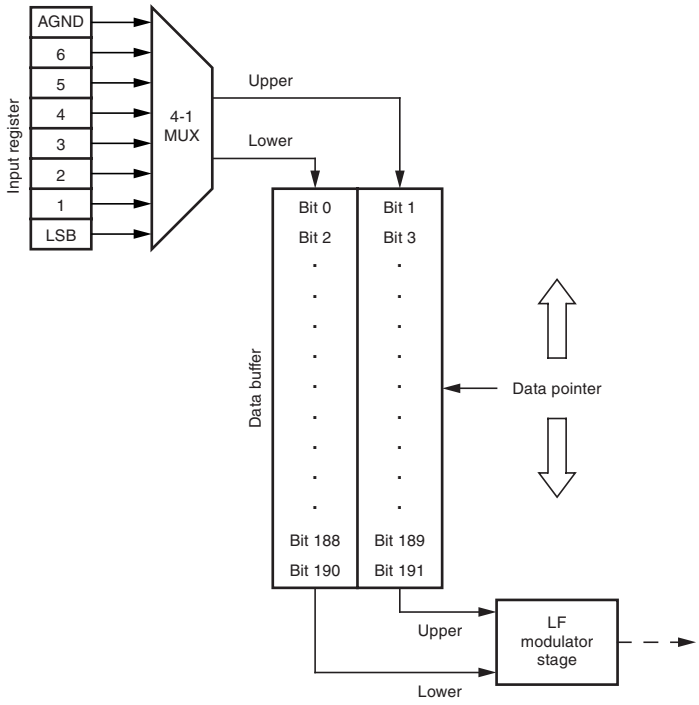
The SPI control logic checks the incoming data for valid commands. If the first data word transmitted by the microcontroller does not match any of the above listed functions, an illegal command fault is detected and written into the fault register. It can be read out with command 9, bit 5 (IC). Note that this fault does not cause a shut down of the power stages.

3.9 LF Data Buffer

The ATA5278 features an 192-bit wide data storage intended to buffer LF data between the microcontroller and the modulator stage. It can be filled with data via the SPI and therefore at high speeds (i.e., up to 1 Mbit/s). The modulator stage then accesses this buffer with the selected LF baud rate and controls the connected LF antenna accordingly. Hence the controller can handle other tasks during the comparatively slow LF data transmission.

The data buffer is structured as a First-In-First-Out (FIFO) system, as can be seen in Figure 3-8 on page 13.

Figure 3-8. Structure Of Internal Data Buffer



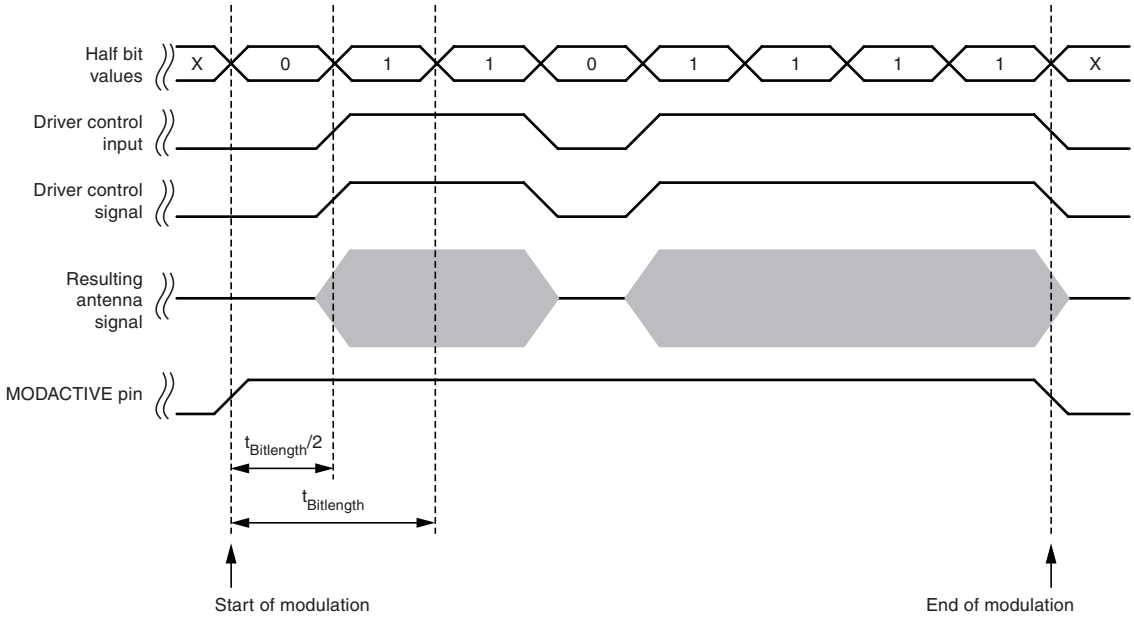
The buffer is structured into two parallel blocks with the same storage capacity. The reason for this is that the LF data is handled as logical (e.g., Manchester coded) bits, where each data is encoded by two so-called half bits. The minimum amount of data which can be written to or read from the buffer is one logical bit, hence two half bits.

After activating the IC from power-down mode or any fault, the data pointer in Figure 3-8 is at the lowest point of the buffer (i.e., bit 190/191). Any write operation will store the data to the position the pointer is pointing at, and moves it upwards one position. The data is always read from the lowest point of the buffer by the modulator stage. Any read operation will cause the data in the buffer to drop down one position, including the data pointer. Any further writes are ignored if the data pointer reaches the upper border of the buffer, and the LF modulator stage stops operation after the pointer has reached the lower border.

3.10 LF Data Modulation

The LF modulator stage of the ATA5278 is fed with data from the LF data buffer. It is started after a successfully received SPI command 11. Two half bits are loaded at a time and brought sequentially to the driver control logic, starting with the half bit labeled lower in Figure 3-8. It is applied for half the period time selected by the LF baud rate selector. Then the half bit labeled upper is applied for the same time. The driver control stage generates a control signal for the power output stages according to the input and the selected modulation mode. The IC has two modulation modes, ASK and PSK. They are selected by the NASK_PSK bit (i.e., bit 0) in control register 1. In ASK modulation mode (NASK_PSK = 0), the IC switches the carrier on and off depending on the value of the half bit applied by the modulator stage, where 1 activates the carrier and 0 deactivates it. So if the carrier is to be activated for a certain time (i.e., continuous wave), a corresponding amount of half bits have to be set to 1 in the LF data buffer. Figure 3-9 on page 14 illustrates this behavior.

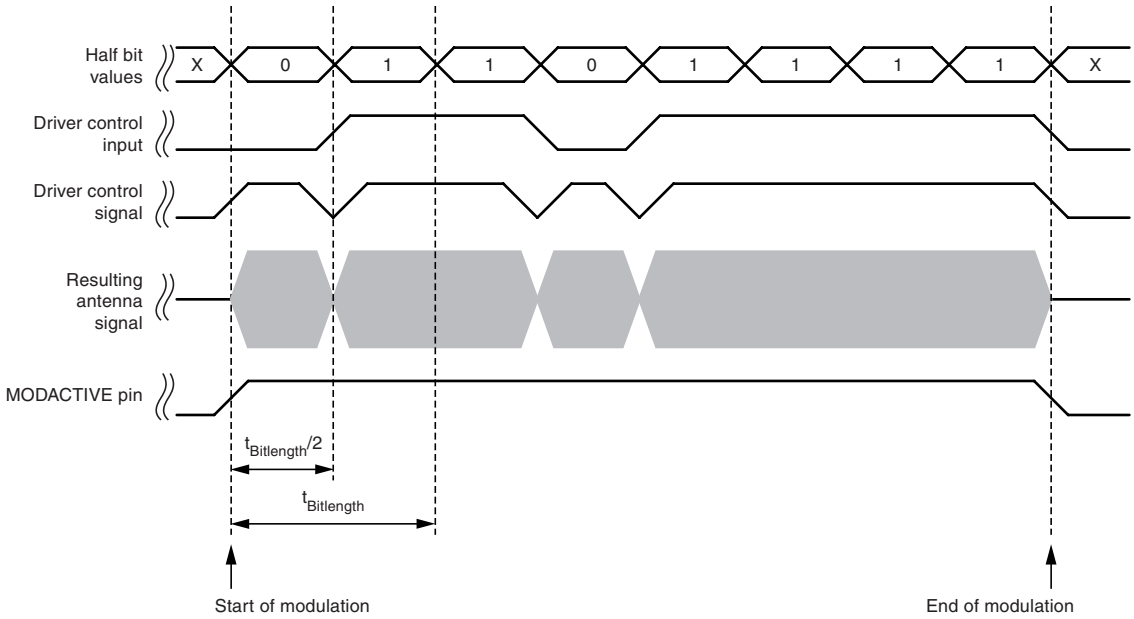
Figure 3-9. LF Data Modulation with ASK



The LF data stream in Figure 3-9 has a length of four logical bits and therefore eight half bits. To get this result, a hex value of 0F6h has to be written into the data buffer via the SPI. The time value $t_{Bitrate}$ is the period of one logical bit, which is defined by the selected data baud rate in configuration register 2. Note that the MODACTIVE pin is active even if the half bit at the modulator stage is “0”.

In PSK mode (NASK_PSK = 1), the phase of the carrier signal is shifted by 180° on any change of the LF data in the buffer. Taking the same data sequence as in the previous example, the diagram changes shown in Figure 3-10.

Figure 3-10. LF Data Modulation with PSK



The carrier signal is now always on as long as the LF data is in the buffer. It is only at the change of the LF data values that the phase of the antenna current is shifted by 180°. For further details, please refer to the section “Driver Stage” on page 16.

An internal timer, derived from the system clock generates the modulation times for the half bits applied to the driver stage. These times depend on the selected LF baud rate in configuration register 2 (i.e., the bits BR0 and BR1). Table 3-2 lists the bit settings and their corresponding timings.

Table 3-2. LF Baud Rate Time Values

BR0 Bit Setting	BR1 Bit Setting	Selected Baud Rate	Time for One Half Bit $t_{Bitlength}/2$	Time for One Logical Bit $t_{Bitlength}$
0	0	1 kbaud	512 µs	1024 µs
1	0	2 kbaud	256 µs	512 µs
0	1	3 kbaud	160 µs	320 µs
1	1	4 kbaud	128 µs	256 µs

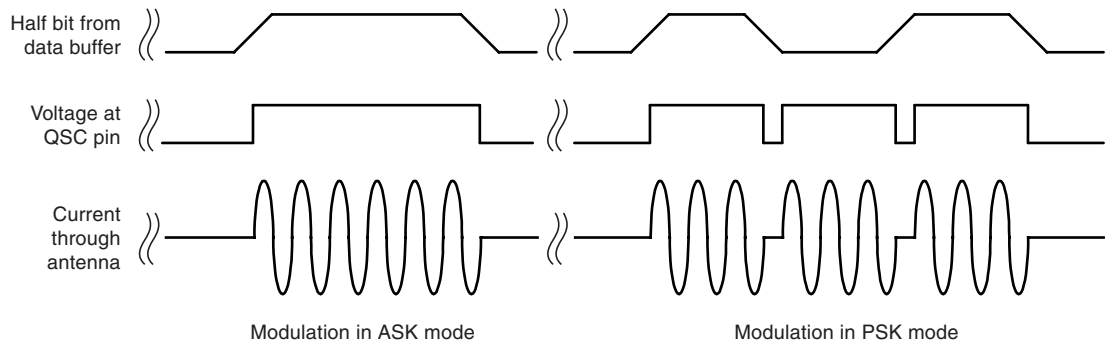
Note that due to synchronization issues, the time for which the LF field is really active in ASK mode when transmitting one half bit might vary by ±8 µs. This is a non-accumulating effect, which means, the transmission time for the complete LF data stream may also vary by ±8 µs, independent of the total amount of logical bits. The same is true for the distance of two phase shifts when transmitting LF data in PSK mode.

If data rates above 2 kbauds are demanded or the PSK modulation mode is selected, the use of an external antenna current loop switch is mandatory. This switch has to be controlled in a defined way which is supported by the ATA5278. For further details on this topic, please refer to the section “QSC Feature” .

3.11 QSC Feature

The Quick Start Control (QSC) feature supports a short oscillation build up and decay time during LF data modulation. An external high-voltage MOS transistor is used as a switch to close and open the current loop of the antenna. By synchronizing this switch to the zero-crossing events of the antenna current, very short build-up and decay times for the LF field, and therefore high data rates can be achieved.

Figure 3-11. QSC Operation



The gate of the external transistor is driven by the QSC pin of the ATA5278. The signal provided here is suited to drive standard MOSFETs (i.e., no logic-level FETs). During power-down mode or a fault shutdown, the external transistor is switched off. Otherwise, this would lead to a conducting state as long as no data modulation takes place. For further information on this pin, please refer to the table “Electrical Characteristics” on page 27.

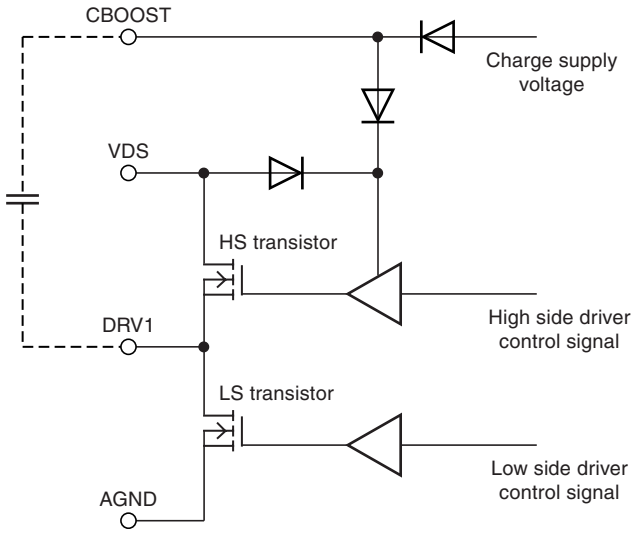
3.12 Driver Stage

The driver stage of the ATA5278 consists of following blocks:

- DMOS half-bridge antenna driver
- Switched Mode Power Supply (SMPS) in boost configuration
- Antenna current sensor for peak value and zero-crossing detection

All these blocks are controlled by the internal driver control logic. The antenna driver stage itself is supplied by the boost converter output voltage, which is applied at the VDS pin. It consists of two power NMOS transistors in half-bridge configuration. As the high-side transistor requires a control voltage above the output voltage (i.e., a voltage above the supply voltage VDS), a bootstrap configuration is implemented. This circuitry requires an external capacitor of 10 nF to 22 nF, connected between the driver output and the CBOOST pin. This capacitor is charged during the time when the low-side transistor is active. As soon as the low-side transistor is switched off and the high-side transistor starts conducting, both the voltage at the DRV1 pin and the CBOOST pin rises, but always with CBOOST being higher than DRV1 and hence being able to provide an appropriate control voltage for the transistor. Figure 3-12 illustrates this boot strapping configuration.

Figure 3-12. Bootstrap Configuration Circuitry



The output signal of the antenna driver stage is of a square wave shape. The duty cycle of this signal is dependant on the selected antenna current. For further details, please refer to the section “Current Adjustment” on page 19.

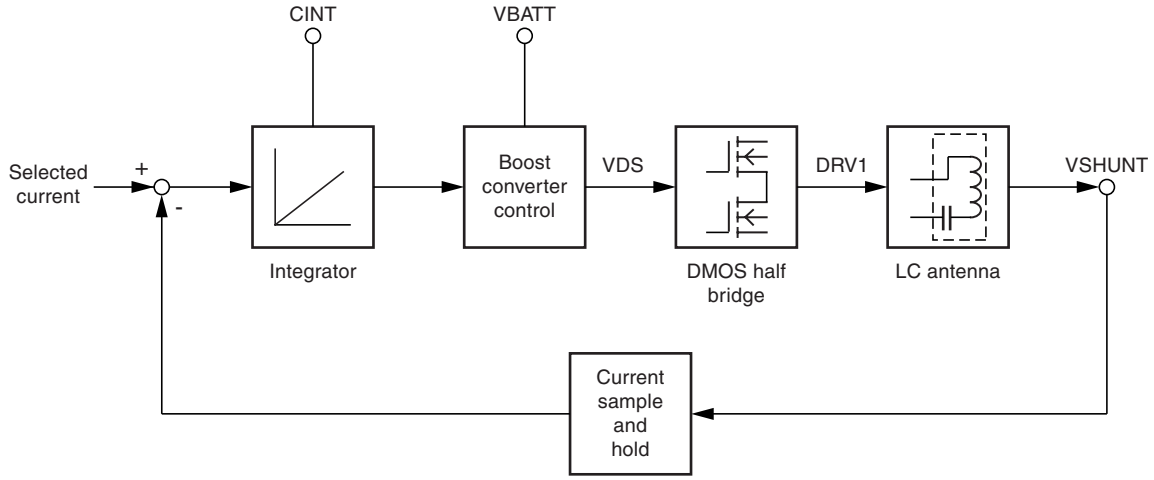
The antenna driver stage and the boost converter are thermally monitored in order to protect them from overheating, and the output pin DRV1 is short-circuit protected by means of current limitation. For further details, please refer to the section “Fault Diagnosis” on page 20.

The current sensor system is equipped with a zero-crossing detector and a sample and hold stage. The zero-crossing detector provides the synchronization signal for the driver control logic, which then calculates the phase shift between the antenna driver output signal and the current flowing through the antenna. Based on this phase information, the sample and hold stage is controlled in order to sample the top point of the input signal, hence the peak current value.

3.13 Current Regulation

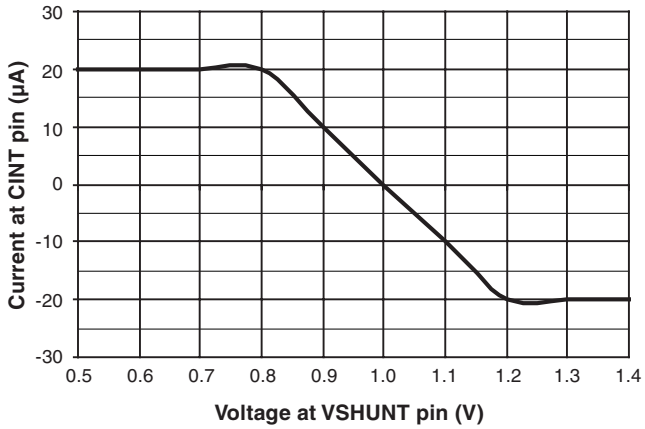
A main feature of the ATA5278 is its ability to generate a stabilized magnetic field with a connected LC antenna, mainly independent of the battery voltage and the frequency mismatch between the driver output frequency and the antenna resonance frequency.

Figure 3-13. Antenna Current Regulation Loop



The input signal for the regulation loop in Figure 3-13 is the selected antenna current, which is defined in configuration register 1. An external shunt resistor of 1Ω, which has to be connected to the VSHUNT pin, is used to measure the current in the LC antenna. As the peak voltage over this resistor is directly linked with the peak current in the antenna and hence the magnetic field strength, this value can be seen as output. This signal is sampled and held by an internal stage controlled by the control logic. The difference of the input signal and the sampled signal then controls an integrator. The parameter of this stage can be influenced with an externally applied charging capacitor connected to the CINT pin. The charging/discharging behavior of the integrator stage is described in Figure 3-14 on page 18.

Figure 3-14. Integrator Output Current on CINT Pin



As can be seen in Figure 3-15 on page 21, a current is charged into, respectively discharged from the external capacitor depending on the voltage at the VSHUNT pin. Note that the shown values for VSHUNT are only valid if maximum antenna current (i.e., 1 A_{peak} when using a shunt resistor of 1Ω) is selected. When the input voltage reaches the desired value (e.g., 1V), no current is flowing through the CINT pin and the voltage over the capacitor is not changing. This voltage influences the output voltage of the boost converter. Note that the lower the voltage on the integration capacitor, the higher the output voltage of the boost converter will be. The maximum output voltage is 40V.

3.14 Boost Converter

The ATA5278 provides the supply current for its driver stage by means of a Switch Mode Power Supply (SMPS) in boost configuration. A low-side switch that charges the inductor, and the therefore needed control circuitry is integrated. The other necessary components such as the inductor, the free-wheeling diode and the charging capacitor have to be applied externally. For further details, please refer to the section "Application Hints" on page 22.

The SMPS control circuitry is in current-mode configuration. This means that the current through the coil charging transistor (i.e., the current through the VL1..3 and the PGND1..3 pins) is measured and compared to a reference current in each switching period. Should the measured value exceed the reference value, the transistor is switched off and the inductor then discharges its energy through the free-wheeling diode to the charging capacitor. The reference current is generated from the voltage on the CINT pin, hence the integrator output voltage.

3.15 Current Adjustment

The maximum reachable output current in the antenna circuit can be calculated as follows:

$$I_{ant,eff} = \frac{V_{DRV} \times \sqrt{2}}{\pi \times |\underline{Z}|} A$$

Here, V_{DRV} is the maximum reachable driver voltage and Z the antenna's impedance (including the R_{DSon} of the QSC MOSFET, the shunt resistor and the driver output resistance). Note when calculating the amount of complex Z, that the antenna driver output frequency (i.e., $f = f_{OSC}/64$) has to be taken into account for the complex parts of the impedance.

The antenna coil current can be adjusted in 16 steps by modifying the IC0..IC3 bits in the configuration register 1. Dependent on the selected current, the duty cycle of the antenna coil driver signal is adapted. This improves the possibility to use one and the same antenna over the whole range of selectable output currents. Table 3-3 provides a list of the current settings for all 16 steps.

Table 3-3. Current Settings

Step	Current [mA]	IC0	IC1	IC2	IC3	P/P ratio
1	$I_{maximum}$/3.597	0	0	0	0	1.25/6.75
2	$I_{maximum}$/3.226	1	0	0	0	1.25/6.75
3	$I_{maximum}$/2.976	0	1	0	0	1.25/6.75
4	$I_{maximum}$/2.604	1	1	0	0	1.25/6.75
5	$I_{maximum}$/2.353	0	0	1	0	1.75/6.25
6	$I_{maximum}$/2.132	1	0	1	0	1.750/6.25
7	$I_{maximum}$/1.984	0	1	1	0	1.75/6.25
8	$I_{maximum}$/1.825	1	1	1	0	1.75/6.25
9	$I_{maximum}$/1.709	0	0	0	1	2.5/5.5
10	$I_{maximum}$/1.57	1	0	0	1	2.5/5.5
11	$I_{maximum}$/1.456	0	1	0	1	2.5/5.5
12	$I_{maximum}$/1.361	1	1	0	1	2.5/5.5
13	$I_{maximum}$/1.256	0	0	1	1	4/4
14	$I_{maximum}$/1.163	1	0	1	1	4/4
15	$I_{maximum}$/1.081	0	1	1	1	4/4
16(1)	$I_{maximum}$	1	1	1	1	4/4

Note: 1. Default

3.16 Fault Diagnosis

The IC contains several fault diagnosis systems to protect itself from destruction and to provide diagnosis information. If a fault at the power stages is detected for a certain debounce time, both the switch mode power supply and the antenna driver stage including the external NMOS transistor (if present) are switched off and the corresponding fault information is written into the status register. Also the LF data buffer is cleared. The fault information can be read out with SPI command 9. In order to restart the operation of the power stages, the status register has to be cleared by transmitting SPI command 2.

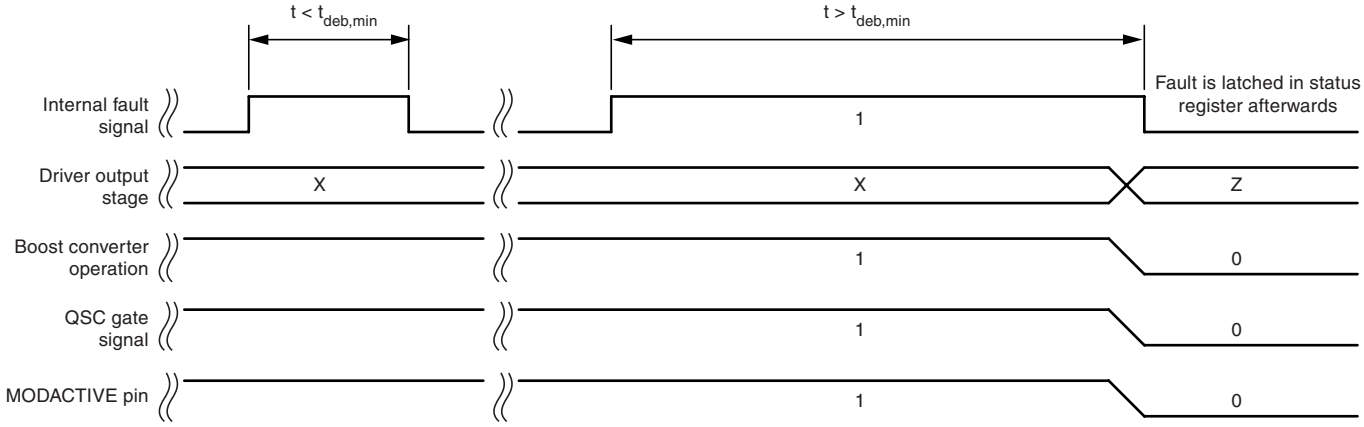
The following protection and diagnosis mechanisms are defined:

- A temperature monitoring system detects critical junction temperatures. Once detected, the debounce timer is started. If the temperature is still above the critical limit after the debouncing time has passed, a fault shutdown is performed.
- A short-circuit protection of the antenna driver output is realized by means of internal shunt-voltage monitoring. Both the high-side and the low-side transistors are equipped with a shunt resistor which provides information about the current flowing through them. If the current through one of the transistors surpasses the internally defined overcurrent level, a current limitation is invoked immediately and the debounce timer is started. Should this condition persist for the whole debouncing time, a fault shutdown is performed.
- The current through the external high-voltage MOSFET is monitored in order to detect short-circuits on the return line of the antenna. Like for the other faults, a debounce timer is started as soon as an overcurrent situation is detected and a fault shutdown is performed after this time has passed.
- The signal at the VSHUNT pin is monitored while the driver stage is active in order to detect a broken antenna connection (i.e., an open load failure). The monitor searches for polarity changes in the signal and starts the fault debouncing timer if it fails to find such changes. A fault shutdown is performed if this fault persists for the whole debouncing time.
- The input register of the SPI is scanned for illegal commands. Note that this kind of fault will cause neither a shutdown of the power stages nor a clearing of the LF data buffer. This diagnosis function is just to provide information about problems on the SPI bus. Also, no debouncing time is applied for this fault.

Some faults, like open load or a short-circuit of the antenna output pin to ground, can only be detected while the driver stage is active (i.e., in modulation mode). As the low-side antenna driver transistor and the QSC transistor are also both active in standby mode, faults concerning these devices are also monitored then. Only during power-down, no fault monitoring is active.

Figure 3-15 on page 21 illustrates the fault shutdown timing sequence.

Figure 3-15. Fault Shutdown Timing



Note: Internal fault signal rises as soon as a fault (overtemperature, short circuit or open load) is detected

Figure 3-15 shows the sequence of a fault shutdown during the antenna driver-stage being active. If a critical condition persists for a time shorter than the debouncing time (e.g., caused by interferences), no shutdown will occur.

The diagnosis bits are based in the status register and are encoded as shown in Table 3-4.

Table 3-4. Diagnosis Bits (Status Register)

Bit Position	Bit Name	Fault Type
0 (LSB)	OT	Overtemperature detected
1	SL	Antenna driver output pin has overload to Ground
2	SH	Antenna driver output pin has overload to VDS (VBATT)
3	OL	Open load detected (no oscillation at VSHUNT pin)
4	CH	Overcurrent at antenna return line (QSC drain input) detected
5	IC	Illegal command in the SPI input register found
6	-	Not defined
7 (MSB)	-	Not defined

3.17 CLKO Output Pin

The clock output pin CLKO of the ATA5278 can be used to supply an on-board microcontroller with a clock signal (either 4 MHz or 8 MHz). This signal is not suited to supply any device beyond the PCB boundaries.

The clock signal is directly derived from the clock source connected to the OSCI/OSCO pins of the ATA5278 and is available as long as the ATA5278 is not in power-down mode. The frequency can be selected with the prescaler (PS) bit in configuration register 2, which is 0 for the full-clock rate ($f_{CLKO} = f_{OSCI}$) or 1 for the half clock-rate ($f_{CLKO} = f_{OSCI}/2$).

3.18 MODACTIVE Output Pin

The MODACTIVE pin of the ATA5278 can be used to directly control a timer/counter stage of the microcontroller. The signal indicates LF data modulation activity. In conjunction with suited timers and counting stages in the microcontroller, it enables the software to precisely know the progress of the LF data transmission. For further details, see Figure 3-9 on page 14 and Figure 3-10 on page 14 in the section "LF Data Modulation" on page 13.

3.19 Internal Supply Unit

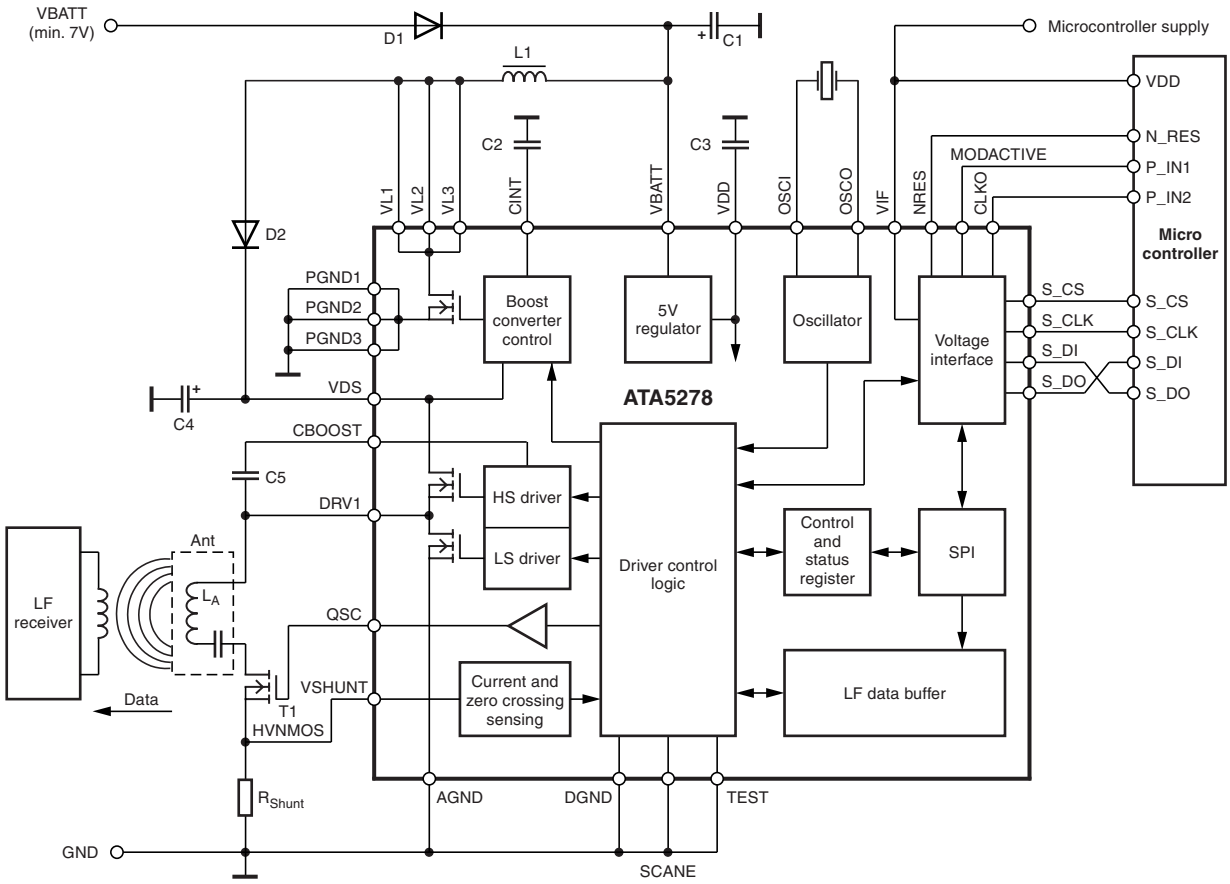
The ATA5278 is equipped with an internal supply unit that provides supply and reference voltages and currents. This unit is directly supplied by the VBATT pin. During power-down mode, only the 5V voltage regulator is active. This regulator requires an external capacitor applied to the VDD pin because during operations high peak currents may occur which must be buffered by the external device. For further details on this issue, please refer to the section "Application Hints" on page 22.

The Power-On-Reset (POR) is also generated in the internal supply section. The VDD voltage level is monitored permanently and compared with the regular output level. As soon as the actual level is lower than the POR threshold, V_{POR}, a reset is triggered and held for at least 30 µs.

3.20 Application Hints

The following Figure 3-16 sketches an application using the ATA5278.

Figure 3-16. Typical Application Circuit With ATA5278



The external components used in this schematic are listed in Table 3-5.

Table 3-5. List of Used Components

Element	Description
D1	Standard diode
D2	Fast Shottky diode, $V_{BR} \geq 50V$, $I_D \geq 2.5$ A
L1	Choke, $I_{SAT} \geq 4A$, $R_{ESR} \leq 50$ mΩ, L = 22 µH
C1	Storage capacitor, C ≥ 220 µF, V ≥ 50 VDC
C2	Ceramic (chip) capacitor, 33 nF ≤ C ≤ 100 nF
C3	Ceramic (chip) capacitor, C ≥ 150 nF
C4	Low ESR capacitor, 4,7 µF ≤ C ≤ 22 µF, V ≥ 50 VDC, $R_{ESR} \leq 0.8\Omega$
C5	Ceramic (chip) capacitor, C = 10 nF, V ≥ 50 VDC
R1	Shunt resistor, R = 1Ω (±1%), $P_{max} \geq 0.6W$
XTAL	Crystal or ceramic resonator, f_{RES} = 8 MHz
T1	High voltage N-channel MOSFET, $V_{DS,max} \geq 600$ VDC, $C_{GS} \leq 2.5$ nF

The following basic hints should be considered when designing an application with the ATA5278.

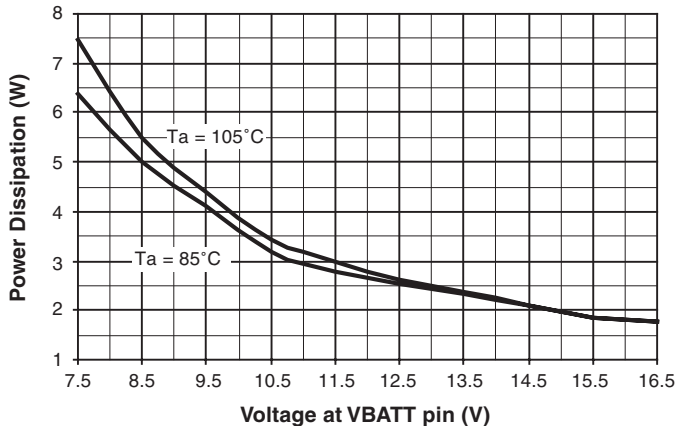
- Principally, the values for the external choke and the storage capacitor used in the switched-mode power supply are not fixed, several performance factors, however, are directly linked to these values. The parameters given in Table 3-5 on page 23 are already optimized to the needs of the internal circuitry and the application.
- The clock supply for the ATA5278 can be either an active clock source connected to the OSCI pin, or a passive device like a crystal or a ceramic resonator. When using a crystal, the prolonged oscillation build-up time (typically up to 1 ms) needs to be considered. Full functionality of the chip will only be available after the oscillation has reached a stable state.
- The external HV-MOSFET for the QSC feature should have a low R_{DSon} value, as this value contributes to the quality factor of the LC antenna circuitry. Furthermore, only standard gate input types may be used. TTL-compatible gate inputs might get destroyed by the driving voltage of the QSC pin.
- The VIF pin must be connected to the supply voltage with which the microcontroller and possible other SPI bus members are driving the SPI bus.
- The VDD pin is intended to be connected to a stabilizing capacitor only. It is not suited for driving any loads.
- The bootstrap capacitor C5 should not exceed values of 22 nF, as the internal charging and clamping circuitry can handle only limited currents.
- The value of the integrator capacitor C2 influences the current regulation speed. The higher the capacitor, the slower the supply voltage for the antenna driver stage and thus the current in the antenna is changed. For more details, please refer to the section "Current Regulation" on page 17.
- The power dissipation of the ATA5278 mainly depends on the supply voltage and the selected antenna current. It is strongly recommended to solder the exposed die pad to the PCB and to provide vias from the top layer (chip soldering side) to the bottom layer, on which a copper plate, as big in size as possible, can dissipate the heat. This plate can be connected to ground.

- The ground pin of R_{SHUNT}, C2, C4 and the AGND pin should be connected together as closely as possible. The same is true for the connection between L1, D2 and VL1..3 and the connection between D2, the positive pin of C4 and the VDS pin.

Note that in any case, the test pins SCANE and TEST must be connected to ground. These pins are for factory test purposes only. For safety reasons, these pins are equipped with a pull-down structure, so that the signals are still defined in case of broken connections. Connecting them to any signal other than ground will result in malfunctions which can lead to the destruction of the chip or the external components.

The power dissipation of ATA5278 is, as already noted, dependant of the supply voltage and the selected antenna current. Assuming an antenna with maximum allowable impedance (i.e., the boost converter will generate 40V output voltage) and the maximum available output current selected (i.e., step 16), the power dissipation of ATA5278 results as shown in Figure 3-17 on page 24

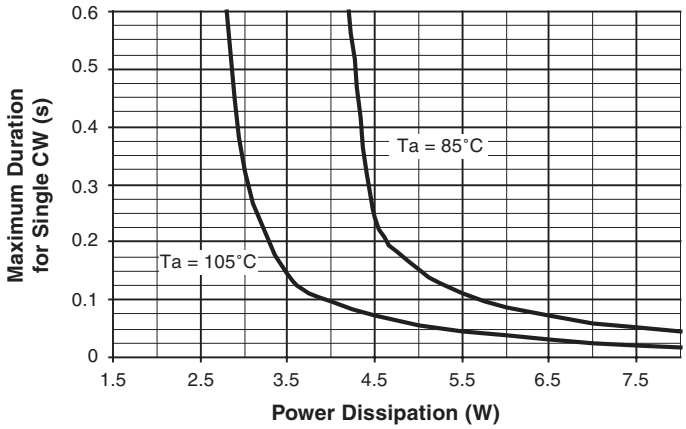
Figure 3-17. Power Dissipation versus Supply Voltage



The static thermal resistance of the chip, soldered onto a PCB can hardly be lowered beneath 30 K/W. Hence, a static operation of ATA5278 is not possible in all cases. But as most applications require only a temporary LF field, the dynamic thermal effects (i.e., the thermal capacitances) are important parameters that must be taken into account.

Figure 3-18 on page 25 shows the maximum reachable LF carrier duration for an example PCB design.

Figure 3-18. Operation Cycle Duration versus Power Dissipation



Note that the upper limit of this diagram (0.6s) is not a design parameter but just for representation reasons. The graphs continue to increase beyond the top line. For this diagram, following parameters have been taken:

- The total thermal resistance is 35 K/W, composed of 10 K/W for the junction-to-case resistance $R_{th,jc}$, 5 K/W for the case-to-copper resistance $R_{th,cpcb}$ and 20 K/W for the copper-to-ambient resistance $R_{th,pcba}$
- For the thermal capacitances, the package with an equivalent capacitance of approximately 15 mJ/K and one PCB copper layer with dimensions of 50 mm × 50 mm × 0.05 mm, resulting in 0.426 J/K have been taken
- The thermal shutdown of the chip triggers at 150°C junction temperature

The thermal resistance $R_{th,jc}$ and the thermal capacitance of the package are fixed values, but everything behind (i.e., the thermal resistance between the solder pad and ambient and the thermal capacitance of the copper layer(s)) depend only on the PCB design.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value[1]	Unit
Supply voltage	V_{BATT}	–0.3 to +44	V
Input voltage (power pins)	V_{INP}	V_{SS} –0.3 ≤ V_{IN} ≤ 46,5	V
Input voltage (interface pins)	V_{IND}	V_{SS} –0.3 ≤ V_{IN} ≤ 5.5	V
Static power dissipation (T_{amb} = 85°C)	P_{tot}	2	W
Emission	EMI	250	V/M
Minimum ESD protection (HBM, 100 pF through 1.5 kΩ)	ESD	1.5 (all pins vs. each other) 4 (pins 5, 6, 7, 8 vs. GND)	kV
Junction temperature	T_J	150	°C
Storage temperature range	T_{stg}	–55 to +150	°C

Note: 1. Voltages are given relative to V_{SS}.

Electrostatic sensitive device.
Observe precautions for handling.

5. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance junction-case	R_{thJC}	10	K/W
Thermal resistance junction-ambient (QFN28)[1]	R_{thJA}	32	K/W

Note: 1. To reach this value, special measures on the PCB have to be taken

6. Operating Range

Parameters	Symbol	Value	Unit
Power supply range	V_{BATT}	7.5 to 16.5	V
Operating temperature range[1]	T_{amb}	-40 to +105	°C

Note: 1. For details, please refer to the section “Application Hints” on page 22 on maximum allowed operation temperature.

7. Electrical Characteristics

6.5V < V_{BATT} < 16.5V, T_{amb} = 25°C unless otherwise specified. All values refer to GND pins. 6V possible with approximately 30% decrease of maximum output power, 28-V operation possible (jump start), but output current stability is not guaranteed in that case.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Power Supply**								
1.1	Supply current in power-down mode	V_{VBATT} = 12V -40°C ≤ T_{amb} ≤ 105°C	25	$I_{SUP,0}$		30	40	µA	A
1.2	Supply current in standby mode	V_{VBATT} = 12V	25	$I_{SUP,1}$	7		9	mA	A
1.3	Internal 5V supply	V_{VBATT} = 12V	24	V_{VDD}	4.7		5.5	V	A
1.4	Supply cap discharging current	V_{VBATT} = 28V V_{VBATT} = 40V	25	I_{DISC1} I_{DISC2}	0.1 3.5		1.5 8	mA mA	A
1.5	Power-down mode driver stage supply current	V_{VBATT} = 12V V_{VDS} = 40V	4	$I_{VDS,0}$			0.5	µA	A
1.6	Standby mode driver stage supply current	V_{VBATT} = 12V V_{VDS} = 12V Pin 7 open	4	$I_{VDS,1}$	1.2		2.2	mA	A
1.7	Voltage interface supply current	V_{VIF} = 5.5V All outputs open	17	I_{VIF}			0.5	µA	A
1.8	Power-on-reset level		24	V_{POR}	0.5		1.05	V	A
2	**I/O Voltage Interface**								
2.1	Interface operation voltage		17	V_{VIF}	3.15		5.5	V	D
2.2	Input high level	–40°C ≤ T_{amb} ≤ +105°C	13, 20-22	V_{INH}	0.6 × V_{VIF}			V	A
2.3	Input low level	–40°C ≤ T_{amb} ≤ +105°C	13, 20-22	V_{INL}			0.3 × V_{VIF}	V	A
2.4	Input hysteresis	–40°C ≤ T_{amb} ≤ +105°C	13, 20-22	$V_{IN,hyst}$	0,03 × V_{VIF}		0,09 × V_{VIF}	V	A
2.5	Input pull-down current	V_{IN} = 5V	14, 15, 20	$I_{IN,pd}$	15		60	µA	A
2.6	Input pull-up current	V_{VIF} = 5V V_{IN} = 0V	13	$I_{IN,pu}$	–20		–3	µA	A
2.7	Input leakage current	V_{VIF} = 5V V_{IN} = 5V V_{IN} = 0V	21, 22	$I_{IN,leak}$	–300		+300	nA	A
2.8	Output source capability	I_{OUT} = –1 mA	12, 16, 23	V_{OUTH}	0.8 × V_{VIF}			V	A
2.9	Output sink capability	I_{OUT} = 1 mA	12, 16, 23	V_{OUTL}			0.2 × V_{VIF}	V	A
2.10	Output off-state leakage current	V_{S_CS} = 0V V_{S_DO} = 2.5V V_{VIF} = 5V	23	I_{ODIS}	–300		+300	nA	A
2.11	Reset prolonging time		13, 20	t_{RESHLD}	135		500	ns	A
2.12	Reset hold time	V_{NRES} ≤ 0.3 × V_{VIF}	13	t_{NRES}	10			ns	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

6.5V < V_{BATT} < 16.5V, T_{amb} = 25°C unless otherwise specified. All values refer to GND pins. 6V possible with approximately 30% decrease of maximum output power, 28-V operation possible (jump start), but output current stability is not guaranteed in that case.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3	**Antenna Driver Stage**								
3.1	High-side driver on resistance	V_{VDS} = 12V V_{CBOOST} = 18V I_{DRV1} = –200 mA T_{amb} = 105°C	4, 5	$R_{DS,HS}$			1.1	Ω	A
3.2	Low-side driver on resistance	V_{VDS} = 12V I_{Load} = 200 mA $T_{amb} \leq$ 105°C	5, 9	$R_{DS,LS}$			1.1	Ω	A
3.3	Switching delay from LS to HS	Trans. between 20% and 80%	5	t_{dLH}	75		150	ns	A
3.4	Switching delay from HS to LS	Trans. between 80% and 20% V_{VDS}	5	t_{dHL}	220		400	ns	A
3.5	HS current limitation	V_{VDS} = 26V R_{Load} = 8.2Ω	5	$I_{LIM,HS}$	1.1		1.8	A	A
3.6	LS current limitation	V_{VDS} = 26V R_{Load} = 8.2Ω	5	$I_{LIM,LS}$	2.0		2.8	A	A
3.7	Bootstrap capacitor clamping voltage	V_{VDS} = 0V I_{CBOOST} = 5 mA	6	$V_{BSOUT,max}$	8		11	V	A
4	**Current Sensing**								
4.1	Zero crossing detection threshold	Rising signal on VSHUNT pin	8	V_{ZC}	8		70	mV	A
4.2	Zero crossing detection delay	Voltage jump on VSHUNT pin from –100 mV to +100 mV	8	t_{dZC}			300	ns	A
4.3	Shunt resistor over-current detection level	R_{SHUNT} = 1Ω	8	I_{QSCSC}	2.3		2.7	A	A
4.4	Nominal operation integrator source current	V_{CINT} = 1.9V V_{VSHUNT} = 750 mV	11	I_{INTSRC}	16		24	µA	A
4.5	Nominal operation integrator sink current	V_{CINT} = 1.9V V_{VSHUNT} = 1250 mV	11	$I_{INTSINK}$	–24		–16	µA	A
4.6	Integrator upper voltage limiting current (sink)	V_{CINT} = 2.8V	11	ILIMUP	40		140	µA	A
4.7	Integrator lower voltage limiting current (source)	V_{CINT} = 1V	11	I_{LIMLOW}	–70		–30	µA	A
4.8	Integrator current de-pendency from antenna current	Current step 16, $V_{VSHUNT,p}$ = 1010 mV	11	dI_{CINT}	600		1400	nA	A
4.9	Integrator current for antenna current step 1	Current step 1, $V_{VSHUNT,p}$ = 278 mV	11	I_{SMPL1}	–0.834		+1.11	µA	A

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7. Electrical Characteristics (Continued)

6.5V < V_{BATT} < 16.5V, T_{amb} = 25°C unless otherwise specified. All values refer to GND pins. 6V possible with approximately 30% decrease of maximum output power, 28-V operation possible (jump start), but output current stability is not guaranteed in that case.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.10	Integrator current for antenna current step 2	Current step 2, $V_{VSHUNT,p}$ = 310 mV	11	I_{SMPL2}	–0.93		+1.24	µA	A
4.11	Integrator current for antenna current step 3	Current step 3, $V_{VSHUNT,p}$ = 336 mV	11	I_{SMPL3}	–1.038		+1.39	µA	A
4.12	Integrator current for antenna current step 4	Current step 4, $V_{VSHUNT,p}$ = 384 mV	11	I_{SMPL4}	–1.152		+1.53	µA	A
4.13	Integrator current for antenna current step 5	Current step 5, $V_{VSHUNT,p}$ = 425 mV	11	I_{SMPL5}	–1.275		+1.6	µA	A
4.14	Integrator current for antenna current step 6	Current step 6, $V_{VSHUNT,p}$ = 469 mV	11	I_{SMPL6}	–1.41		+1.66	µA	A
4.15	Integrator current for antenna current step 7	Current step 7, $V_{VSHUNT,p}$ = 504 mV	11	I_{SMPL7}	–1.51		+1.72	µA	A
4.16	Integrator current for antenna current step 8	Current step 8, $V_{VSHUNT,p}$ = 548 mV	11	I_{SMPL8}	–1.44		+1.84	µA	A
4.17	Integrator current for antenna current step 9	Current step 9, $V_{VSHUNT,p}$ = 585 mV	11	I_{SMPL9}	–1.52		+2.0	µA	A
4.18	Integrator current for antenna current step 10	Current step 10, $V_{VSHUNT,p}$ = 637 mV	11	I_{SMPL10}	–1.67		+2.15	µA	A
4.19	Integrator current for antenna current step 11	Current step 11, $V_{VSHUNT,p}$ = 687 mV	11	I_{SMPL11}	–1.76		+2.36	µA	A
4.20	Integrator current for antenna current step 12	Current step 12, $V_{VSHUNT,p}$ = 735 mV	11	I_{SMPL12}	–1.87		+2.55	µA	A
4.21	Integrator current for antenna current step 13	Current step 13, $V_{VSHUNT,p}$ = 796 mV	11	I_{SMPL13}	–1.98		+2.8	µA	A
4.22	Integrator current for antenna current step 14	Current step 14, $V_{VSHUNT,p}$ = 860 mV	11	I_{SMPL14}	–2.06		+3.1	µA	A
4.23	Integrator current for antenna current step 15	Current step 15, $V_{VSHUNT,p}$ = 925 mV	11	I_{SMPL15}	–2.16		+3.4	µA	A
4.24	Integrator current for antenna current step 16	Current step 16, $V_{VSHUNT,p}$ = 1000 mV	11	I_{SMPL16}	–2.2		+3.8	µA	A

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7. Electrical Characteristics (Continued)

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.25	Antenna current regulation precision				–6		+6	%	C
5	**Boost Converter**								
5.1	Boost switch transistor leakage current	V_{VL1-3} = 18V –40°C ≤ T_{amb} ≤ +105°C	26-28	$I_{VL,Leak}$			1	µA	A
5.2	Boost switch transistor on resistance	$I_{VL1..3}$ = 1A T_{amb} ≤ 105°C	26-28, 1-3	R_{DSon}			270	mΩ	A
5.3	Switching frequency		26-28	f_{Boost}			f_{OSCI}/32	Hz	D
5.4	Minimum switch-on time per period	f_{Boost} = 250 kHz	26-28	t_{DCL}	0		100	ns	A
5.5	Maximum switch-on time per period	f_{Boost} = 250 kHz	26-28	t_{DCH}	3750		3910	ns	A
5.6	Switching-on signal fall time	$I_{VL1..3}$ = 0.4A	26-28	$t_{f,Boost}$	15		80	ns	A
5.7	Switching-off signal rise time	$I_{VL1.3}$ = 0.4A	26-28	$t_{r,Boost}$	20		80	ns	A
5.8	Switch-off current threshold	I_{VL} = 1.25A	11	V_{CINT1}	2.2		2.8	V	A
5.9	Switch-off current slope compensation	V_{CINT} = V_{CINT} from meas. 5.8	26-28	dI_{CUT}/dt		1.6		A/µs	A
5.10	Overvoltage shut-down level		4	V_{VDSLIM}	41		46.5	V	A
5.11	Overtemperature shut-down level (junction temperature)	T_{amb} = 105°C	26-28	$T_{OTBoost}$	150		170	°C	C
6	**QSC Transistor Driver**								
6.1	Maximum output voltage	V_{VDS} = 40V no DC load on pin QSC, –40°C ≤ T_{amb} ≤ +105°C	7	$V_{Q,max}$	11		16	V	A
6.2	High-side output voltage under load	V_{VDS} = 12V I_{QSC} = –40 mA –40°C ≤ T_{amb} ≤ +105°C	7	$V_{Q,min}$	8.5		12	V	A
6.3	Low-side output voltage under load	V_{VDS} = 40V I_{QSC} = 40 mA –40°C ≤ T_{amb} ≤ +105°C	7	$V_{Q,off}$	0.2		0.5	V	A
6.4	Switch-on signal rise time	V_{VDS} = 8V C_{Load} = 2 nF 10% to 90% transition	7	$t_{r,QSC}$	100		200	ns	A

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7. Electrical Characteristics (Continued)

6.5V < V_{BATT} < 16.5V, T_{amb} = 25°C unless otherwise specified. All values refer to GND pins. 6V possible with approximately 30% decrease of maximum output power, 28-V operation possible (jump start), but output current stability is not guaranteed in that case.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6.5	Switch-off signal fall time	V_{VDS} = 8V C_{Load} = 2 nF 90% to 10% transition	7	$t_{f,QSC}$	40		90	ns	A
6.6	Bootstrap capacitor charging voltage	V_{VDS} = 12V I_{CBOOST} = –10 mA	6	$V_{BSOUT,min}$	5.5		10	V	A
7	**SPI**								
7.1	Clock frequency		21	f_{S_CLK}			f_{OSCI}/8	Hz	D
7.2	Clock signal high time		21	$t_{S\_CLK,h}$	4/f_{OSCI}			s	D
7.3	Clock signal low time		21	$t_{S\_CLK,l}$	4/f_{OSCI}			s	D
7.4	Input signal setup time		22	$t_{DI,setup}$			100	ns	D
7.5	Input signal hold time		22	$t_{DI,hold}$			100	ns	D
7.6	Output signal enable time		23	$t_{DO,enable}$			100	ns	D
7.7	Output signal disable time		23	$t_{DO,disable}$			100	ns	D
7.8	Output signal delay time		23	$t_{DO,delay}$			100	ns	D
8	**Oscillator**								
8.1	Input frequency range	Ceramic resonator, crystal or external clock source	19	f_{OSCI}		8		MHz	D
8.2	Feedback resistance	–40°C ≤ T_{amb} ≤ +105°C	18, 19	$R_{FB,OSC}$	140		400	kΩ	A
8.3	Startup sink current	V_{OSCI} = 5V V_{OSCO} = 4V	18	I_{L2}	2.0		3.7	mA	A
8.4	Operation sink current	V_{OSCI} = 5V V_{OSCO} = 3V	18	I_{L1}	1.1		1.8	mA	A
8.5	Startup source current	V_{OSCI} = 0V V_{OSCO} = 1.45V	18	I_{H2}	–3.7		–2.0	mA	A
8.6	Operation source current	V_{OSCI} = 0V V_{OSCO} = 0.8V	18	I_{H1}	–2.0		–1.2	mA	A
8.7	Maximum OSCI low-time for clock driver to stay in operation mode	V_{OSCI} < 0.5 × V_{VDD}	19	$t_{LOW,max}$			660	ns	D
8.8	Oscillator input pull-down current	Power-down mode, V_{OSCI} = 5V V_{OSCO} = 5V	19	$I_{OSCI,PD}$	100		250	µA	A
8.9	Switch-on debounce time after clock signal is stable			t_{deb}		192/f_{OSC}		s	D

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7. Electrical Characteristics (Continued)

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9	**Fault Diagnosis**								
9.1	Debounce time for driver stage faults	DRV1 short-circuit to VBATT or GND	5	$t_{deb,min}$	120			µs	D
9.2	Debounce time for antenna return line faults	QSC input short-circuit to VBATT open load	8	$t_{deb,min}$	120 160			µs	D
9.3	Debounce time for overtemperature fault			$t_{deb,min}$	20		32	µs	D

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8. Soldering Recommendations

Parameters	Symbol	Value	Unit
Maximum heating rate	T_D	1 to 3	°C/s
Peak temperature in preheat zone	Z_{PH}	100 to 140	°C
Duration of time above melting point of solder	t_{MP}	Minimum 10 Maximum 75	s
Peak reflow temperature	T_{Peak}	220 to 225	°C
Maximum cooling rate	T_{rPeak}	2 to 4	°C/s

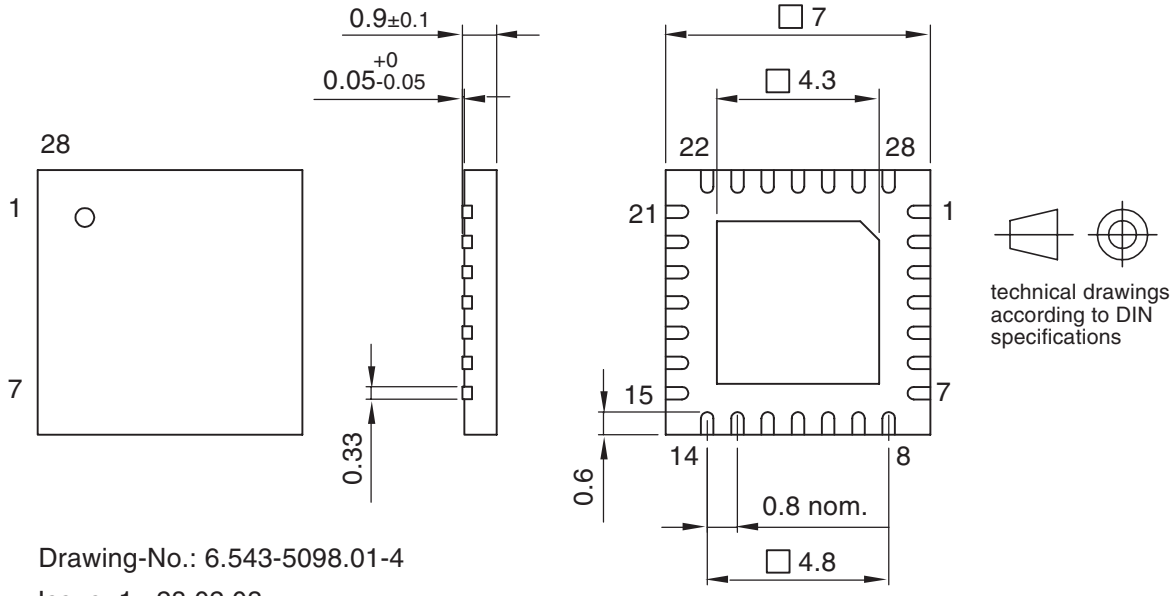
9. Ordering Information

Extended Type Number	Package	Remarks
ATA5278-PKQI	QFN28	7 mm × 7 mm, taped and reeled, Pb-free

10. Package Information

Package: QFN 28 - 7 x 7
Exposed pad 4.3 x 4.3
(acc. JEDEC OUTLINE No. MO-220)
Dimensions in mm

Not indicated tolerances ± 0.05



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11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4832D-RKE-12/07	• Put datasheet in the newest template

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
auto_control@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature